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Satellite B-ISDN Traffic Analysis<sup>1</sup>

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## Summary

This paper reports on the impact of asynchronous transfer mode (ATM) traffic on the advanced satellite broadband integrated services digital network (B-ISDN) with on-board processing. Simulation models have been built to analyze the cell transfer performance through the statistical multiplexer at the earth station and the fast packet switch at the satellite. The effectiveness of ground ATM cell preprocessing has been established, as well as the performance of several schemes for improving the down-link beam utilization when the space segment employs a fast packet switch.

## 1. Introduction

With its flexibility in bandwidth allocation for various traffic types, channel structures, and synchronization rates, B-ISDN is a promising technique to accommodate diverse current and future services and traffic. Potential applications for satellite B-ISDN include video distribution services, live newscast/broadcast, science data distribution, supercomputer networking, private network, and trunking. Providing these services necessitates the development of new network architectures, advanced on-board processing, and special processing at the earth station.

Two types of transfer mode can accommodate B-ISDN services: circuit switching and fast packet switching. Fast packet switching is more effective than circuit switching in providing services for multirate, multimedia, and bursty data due to its statistical multiplexing and inherent dynamic bandwidth allocation properties. Also the current trend in the transmission of telecommunications traffic is based on packet communications such as frame relay/frame switching, ATM, and consultative committee for space data systems (CCSDS). An on-board fast packet switch gives the satellite the flexibility to handle services with different traffic characteristics and requirements, and to provide higher transmission throughputs than circuit switching. Also, an on-board fast packet switch with multiple spot beam operation gives the satellite network an advantage over the terrestrial network in providing multicast services. In this paper, the earth station is assumed to be equipped with ATM interfaces and the space segment with a fast packet switch.

For ATM, the packet size is fixed and each packet, called a cell, consists of a 5-byte header and 48-byte information payload. In ATM cells, routing information consists of a 24-bit virtual path identifier and virtual channel identifier (VPI/VCI) at the user network interface (UNI) and a 28-bit VPI/VCI at the network node interface (NNI). To reuse VPI address space and avoid VPI retranslation on-board, the satellite virtual packet (SVP) concept is introduced. SVPs are created by appending a header, used only within the satellite network and containing a routing tag for the on-board switch, to one cell or a group of cells destined to the same down-link beam.

Since the satellite resources are bandwidth limited, the design focus is increase down-link beam utilization. To achieve this objective, one approach is to increase the throughput of the on-board fast packet switch. Different fast packet switch architectures have been proposed to improve the switch throughput [1]. Two fast packet switching architectures are considered in this paper: the input queueing fast packet switch with a nonblocking switching fabric and the output queueing fast packet switch with a nonblocking switching fabric.

For the input-queueing fast packet switch, the throughput is constrained by the head of line blocking problem. Three schemes to improve the throughput have been investigated: increasing the input buffer size, increasing the searching depth of the input queue to resolve the output contention, and increasing the switch speed. For the output-queueing fast packet switch, the incoming packets are not stored in the input buffers; the (banyan-type) switch must operate  $N$  times faster than the line speed to avoid the output contention problem, where  $N$  is the switch size.

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The focus of this paper is performance analysis of the ATM cells (cell delay jitter and cell delay distribution) through the multiplexer at the earth station and the fast packet switch at the satellite using the SVP concept.

## 2. Satellite Virtual Packets

SVPs are created by appending a header to one cell or a group of cells destined to the same down link beam at the earth station (see Figure 1) for unified routing, control, and management. The header of the SVP is termed the satellite virtual label (SVL).

There are three possible formats for grouping the cells at the earth station: fixed size packets, variable size packets, or single cells. In this paper, the fixed size approach for SVPs has been adopted.

The necessary fields of the SVL are proposed to consist of the switch routing tag, sending earth station address, receiving earth station address, quality of service (QOS) field, control field, and cyclical redundancy check.

A larger SVP has a higher transmission capacity utilization. It also increases the packet interarrival time and the packet slot time, which decreases the speed requirement for on-board SVP processing. However, a larger SVP has a longer packetization delay, longer end-to-end delay, and worse delay jitter. It also results in a larger buffer requirement and increases the number of bits of the packet payload in error. In this paper, the performance of SVPs of different sizes are compared and analyzed in terms of delay through the satellite B-ISDN.

The tradeoff study between SVP processing and cell processing in the satellite B-ISDN has been omitted due to the page limitations.

## 3. Performance Analysis of SVP Ground Preprocessing and On-Board Processing

In this subsection, the cell delays through a multiplexer and a fast packet switch are collected from the simulation models to study the performance of SVP transmission through the satellite B-ISDN.

A brief description of the satellite B-ISDN simulation model (see Figure 2) is given below. The number of earth stations, up-link beams, and down-link beams is assumed to be the same as the size of the on-board switch. Each earth station is interfaced with five UNIs. These five input lines at the earth station have the same transmission rate of 155.52 Mbit/s. The up-link and down-link access schemes use time-division multiplexing (TDM). The link transmission rate is also 155.52 Mbit/s. The on-board switch speed is (speedup factor \* 155.52 Mbit/s). The cell slot time is equal to  $2.726 \times 10^{-6}$  s when the transmission rate is 155.52 Mbit/s. In the figures, CDJ designates the cell delay jitter,  $u$  the link utilization,  $d$  the checking depth, and  $s$  the speedup factor of the switch.

### 3.1 SVP Transmission vs Cell Transmission at the Earth Station

Earth stations in the satellite B-ISDN are interfaced with different UNIs and network node interfaces (NNIs). To increase the transmission link efficiency and share the satellite transmission link among different users, the advanced earth station functions as a statistical multiplexer. At the earth station, it is assumed that the buffer size of the multiplexer is infinite; therefore, its cell loss ratio is zero.

The first set of results illustrates the effect of different SVP sizes on the cell delay performance and the buffer size requirements at the earth station for different transmission link utilizations and numbers of down-link beams.

Figure 3 shows the cell delay jitter of the statistical multiplexer at the earth station for different SVP sizes, output link utilizations, and numbers of down-link beams. As shown in this figure, for different sizes of SVPs, the increase in of the cell delay is proportional to the size of the SVPs. Based on these results, SVPs should be small if cell delay is an important QOS parameter. Also as shown in this figure, when the output link utilization is higher, the delay performance of SVP transmission improves while that of single-cell transmission degrades. That is, when the output link utilization is higher, the probability that an SVP will be filled with cells destined to the same down-link beam within a given time is also higher. Hence, the delay performance of the SVPs improves when the output link utilization is higher. Basically, the cell delay for the SVPs consists of three elements: the packetization delay (the time required to fill the SVP with cells), the waiting time in the queue, and the transmission time. From Figure 3, most of the delay for the SVPs occurs during the packetization process.

It can be seen from Figure 3 that the cell delay for SVP transmission is proportional to the number of down-link beams. As previously mentioned, the cell delay for SVP transmission is dominated by the packetization delay. If there are more down-link beams, the filling rate for each SVP destined to a different down-link beam is reduced when the output link utilization is kept constant.

In conclusion, the delay performance of cells for single-cell transmission is determined by the waiting time in the queue for transmission, i.e., the queueing delay. The delay performance of the cells for SVP transmission is largely determined by the packetization delay. This implies that, if the SVP transmission concept is used for the satellite network, the satellite network link must be operated at a very high utilization (above 80 percent) therefore, the on-board fast packet switch throughput must also be higher than 8 percent.

Figure 4 shows the cell delay probability mass function for different SVP sizes and link utilization when the number of down-link beams is 80. From the cell delay distribution, the buffer size requirement for the earth station to achieve a certain cell loss ratio can be derived. For example, for a 4-cell SVP and utilization equal to 0.6, the probability that the cell delay is 400 ms is about  $10^{-4}$ . Hence, to have a cell loss ratio of  $10^{-4}$ , the buffer size required for the statistical multiplexer is about 37 SVPs. With higher utilization, the cell delay distribution curves of the SVPs approach the cell delay distribution curves for single-cell transmission.

### 3.2 On-Board Fast Packet Switch Performance

For the on-board fast packet switch, since the mass and power are the constrained design factors for satellites, the buffer size of the switch must be finite. Also, since the satellite communications system is both power and bandwidth limited, the down-link beam resource must be used very efficiently. One way of increasing the down-link beam utilization is to increase the throughput of the switch. The on-board fast packet switch architectures are assumed to be banyan-type switching networks. The switching fabric is assumed to be unbuffered and point-to-point nonblocking. Since output blocking is unavoidable for a packet switch, it is assumed that packets are buffered either at the input ports or at the output ports.

#### 3.2.1 Input Buffering

In this scheme, the packets are buffered at the input ports. The throughput of a switch with first-in first-out (FIFO) input queue is limited by the head of line blocking problem. It has been shown that the theoretical throughput for the input buffering nonblocking point-to-point switch with infinite buffer size is about 0.58 [2]. Head of line blocking is a side effect of output blocking. This is, if one packet at the head of queue cannot be transmitted due to output blocking, this packet hinders the delivery of the next packet in the queue due to the FCFS nature of the queue, even though the next packet can be transmitted to the destination without any blocking. Three schemes have been studied to improve the throughput of the switch. The first is to increase the buffer size. Intuitively, the larger the buffer size, the better the packet loss ratio, but the worse the delay performance. The second method is to use a non-FIFO queue. If the first packet is blocked due to output blocking, the scheduling algorithm will also examine the packets at the back of the first packet. The number of packets examined each time depends on the preset window size or the checking depth. For a normal FIFO operation, the checking depth is 1. The third method is to operate the switch at a speed higher than the link speed.

##### 3.2.1.1 Increasing Buffer Size

The buffer requirement for the on-board switch is determined by measuring the cell delay distribution using infinite buffer size. From the delay distribution, the buffer size requirement for a specific cell loss ratio can be calculated as given in the example in Subsection 3.1. Figure 5 shows the cell delay jitter for different SVP sizes through the on-board switch. The delay degradation of a larger SVP through the fast packet switch is much less than that through the multiplexer at the earth station because, unlike the multiplexer, no packetization process is required at the switch. When the utilization is low, the single-cell delay performance is better than the SVP delay performance because the SVP transmission time through the switch is  $n$  times longer than the cell transmission time, where  $n$  is the size of the SVP. In general, under the same conditions, the packet delay through a switch for a packet of size  $n$  cells is  $n$  times larger than that for a single cell.

From Figure 5, when the link utilization is higher (approaching the 0.6 switch throughput of an  $8 \times 8$  switch), the cell delay performance degrades much more quickly than the SVP delay performance. Eventually, the SVP delay performance is better than the single-cell delay performance because the process of formatting cells into SVPs at the

earth station disturbs the traffic pattern. Note that the traffic pattern coming to the simulated satellite network is assumed to be random. Under this scenario, the probability that  $n$  SVPs destined to the same destination beam arrive at the input port of the switch continuously is less than that of  $n$  cells, where  $n > 1$ . Hence, output contention of the on-board switch is reduced. This discovery is useful if the traffic coming to the earth station can be assumed to be random, as in the case of packet-switched traffic. In this case, the throughput of the on-board switch is increased by formatting the SVP at the earth station since the output contention problem of the switch is reduced.

The cell delay distribution for different SVP sizes and different link utilizations is shown in Figure 6. The results show that when the utilization is low, the single-cell packet has the best performance. When the utilization is high, the SVP with size 2 has the best delay performance. This is because, when the link utilization is low, the packets are usually very sparse on the transmission link; hence, the packet transmission time through the switch dominates the delay performance. When the link utilization is high, the probability of continuous arrivals of packets with the same destination at the input port (called  $P_C$ ) intensifies the output contention problem. When  $P_C$  is high, the average queue length is higher and each packet will experience a higher queueing delay. However, when the SVP size increases,  $P_C$  decreases. With a smaller  $P_C$ , the average queue length is reduced. Although the average queue length is reduced, the average queue delay is the product of the average queue length and the packet service time. Therefore, there is a tradeoff between the packet service time through the switch and the SVP size to optimize the cell delay under the same link utilization. In conclusion, the cell delay distribution through the switch is determined by two factors: the packet transmission delay and the probability of continuous arrivals of packets with the same destination at the input port.

From the cell delay distribution provided in Figure 6, using the extrapolation scheme the buffer size required to achieve  $CLR 10^{-9}$  is around 100 for single-cell transmission when the link utilization is only 0.55. To achieve the same CLR, the buffer size requirement will be increased exponentially when the link utilization approaches 0.6 switch throughput. Therefore, increasing the buffer size is not effective for improving the throughput of the fast packet switch, and it is not appropriate for the satellite environment.

### 3.2.1.2 Non-FIFO Queue

Using a non-FIFO queue with a checking depth of 2, the switch throughput can be increased from 0.6 to 0.73. Using a non-FIFO queue with a checking depth of 3, the switch throughput can be increased from 0.6 to 0.79. The switch throughput improvement decreases when the checking depth increases.

The cell delay jitter of the switch for checking depths of 2 and 3 is depicted in Figure 7. Compared this figure with Figure 4, the non-FIFO queue is an effective scheme for increasing the down-link beam utilization. In implementation, the maximum checking depth is determined by the processing speed of the routing tag of each packet at the input port queue. Since the scheduling algorithm must operate at the same speed as the switch and the number of packets processed by the scheduling algorithm is proportional to the switch size, the maximum checking depth allowed for a smaller switch is larger than that of a larger switch. Since the size of the on-board switch is between  $O(10)$  and  $O(100)$ , the non-FIFO queue with a preset checking depth is proper for satellite application.

### 3.2.1.3 Increasing Switch Speed

The third scheme is to operate the switch at a speed faster than the link speed so that more incoming packets can be processed by the switch in one packet slot time ( $\text{pkt size/link speed}$ ) and the output contention problem is reduced. If the output contention problem is reduced, the input queueing delay is also reduced. In this scheme, since the switch speed is greater than the down-link speed, to effectively improve the down-link beam utilization, buffering is required at the output ports to hold the packets. The output queue performs as a statistical multiplexer and the speed of the multiplexer is the same as the down-link speed.

It is possible to combine the non-FIFO queue scheme and the speedup scheme so that the tradeoff among throughput, delay, and hardware cost can be optimized. Two configurations simulated to show the effect of speedup: the first has a speedup factor of 1.5 and checking depth of 1, and the second has a speedup factor of 1.25 and checking depth of 2. Note that the maximum achievable throughput for both configurations is around 0.9.

The cell delay jitter of the switch for both configurations is depicted in Figure 8. The single-cell and SVP delay distributions for both configurations with link utilization as a parameter are provided in Figures 9 and 10, respectively. For single-cell transmission, when the utilization is less than 0.85, the delay performance for both

configurations is about the same. When the utilization approaches 0.9, the first configuration performs better. This is because the packet transmission time through the switch for a speedup factor of 1.5 is less the packet transmission time for a speedup factor of 1.25. For SVP transmission, the delay performance is about the same for both configurations and all utilizations. Note, as previously mentioned, that there is a tradeoff between the packet service time through the switch and SVP size to optimize the packet delay. Therefore, the combination scheme using speedup and a non-FIFO queue, is adequate for single-cell transmission and lower utilization, and it is appropriate for SVP transmission for all utilizations.

### 3.2.2 Output Buffering

In this approach, the packets are buffered at the output ports. To resolve output contention, either the switching fabric must operate at a speed faster than the line speed, as in the case of the banyan-type network, or there must be disjoint path between any input-output pair and the output port must have multiple buffers such as the knockout switch [3]. In this paper, only the banyan-type switch is considered. If the switching speed is  $N$  times faster than the line speed (where  $N$  is the size of the switch), all the packets destined to the same output port during the same slot time can be buffered at the output port. However, this approach is feasible only if the link speed is low and the switch size is small. In conclusion, it is not feasible to use output buffering alone to increase the throughput of the banyan-type switch.

## 4. Concluding Remarks

Based on the performance analysis of SVP transmission through the earth station, to fully utilize the SVP concept without affecting the delay quality, the up-link and down-link must operate at a very high utilization (above 80 percent). In such a configuration, the packet delay at the earth station is minimized. It is also found that the SVP formatting at the earth station reduces the probability of continuous arrivals of packets with the same destination at the input port. The result has shown to be effective in reducing output contention of the on-board switch. It suggests that spacing is one of the necessary requirements for satellite B-ISDN congestion control. The spacing process is one of the traffic shaping functions used to ensure that cell streams coming into the network do not exceed the negotiated value between the subscriber and the network. The spacing mechanism does not send the packets with the same destination back by back, since the peak value for this stream is the same as the satellite transmission link. Other packets with different destinations can be inserted between two packets with the same destination. The result of spacing is that output contention of the on-board switch is reduced.

To provide high up-link and down-link utilization within the satellite network, the on-board fast packet packet throughput must be greatly improved. Several schemes have been examined in the paper. Increase buffer size is not effective for the satellite environment. The non-FIFO queue with a preset checking depth at the input port to resolve HOL blocking has shown to be effective. However, the throughput improvement is still very limited since it is not practical to use a large checking depth. To significantly increase the throughput, the speedup scheme must be used. It has been found that the non-FIFO queue in conjunction with the speedup scheme can significantly increase the throughput of the switch at a reasonable hardware cost. Therefore, the combination of input queueing, a non-FIFO queue with a preset checking depth, speedup, and output queueing optimizes the performance of the switch and the hardware cost.

This paper has analyzed single-cell and SVP performance through the satellite B-ISDN for point-to-point traffic only. Extension of this work to point-to-multipoint traffic is currently under study.

## References

- [1] F. A. Tobagi, "Fast Packet Switch Architectures for Broadband Integrated Services Digital Networks," *Proc. IEEE*, Vol. 78, No. 1, pp. 133–167, Jan. 1990.
- [2] M. Karol, M. Hluchyj, and S. Morgan, "Input vs Output Queueing on a Space-Division Packet Switch," *IEEE Trans. on Communications*, Vol. 35, pp. 1347–1356, Dec. 1987.
- [3] U. Yeh, M. Hluchyj, and A. Acampora, "The Knockout Switch: A Simple, Modular Architecture for High-Performance Packet Switching," *IEEE JSAC*, Vol. 5, pp. 1274–1283, Oct. 1987.

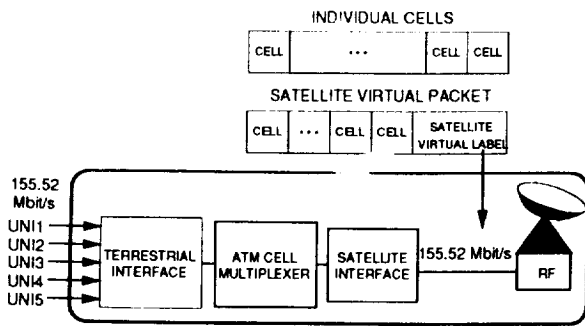


Figure 1: ATM Earth Station Configuration

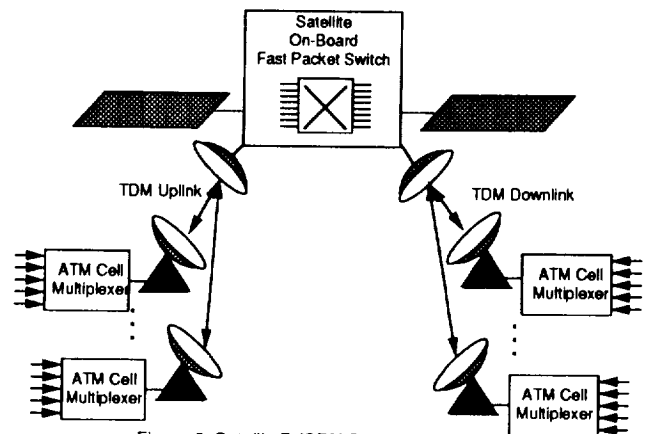


Figure 2: Satellite B-ISDN Simulation Model

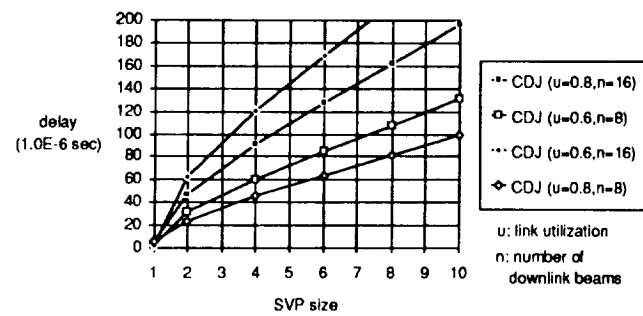


Figure 3: Cell Delay Jitter Versus SVP Sizes for Different Link Utilization and Number of Downlink Beams

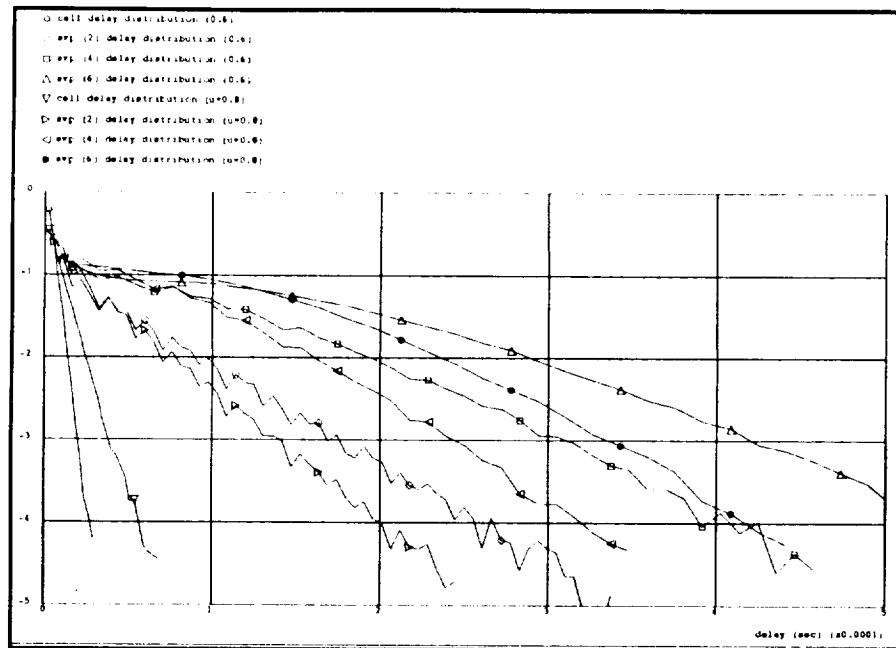


Figure 4: Cell Delay Distribution through the Earth Station for Different SVP Sizes and Link Utilization

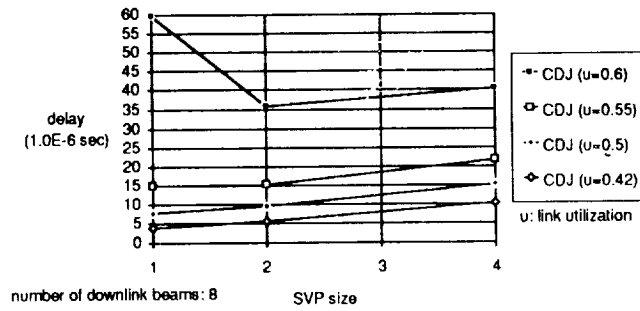


Figure 5: Cell Delay Jitter Versus SVP Sizes for Different Link Utilization

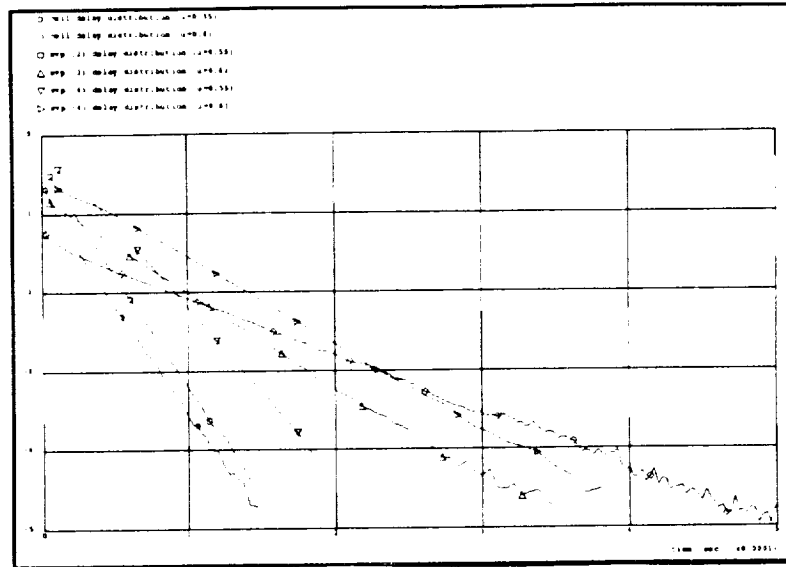


Figure 6: Cell Delay Distribution through the On-Board Switch for Different SVP Sizes and Utilizations

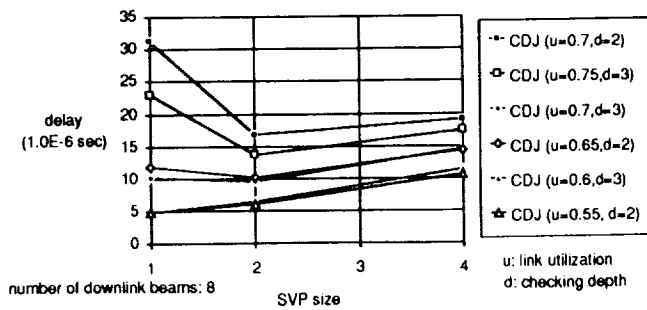


Figure 7: Cell Delay Jitter Versus SVP Sizes for Different Link Utilization and Checking Depth

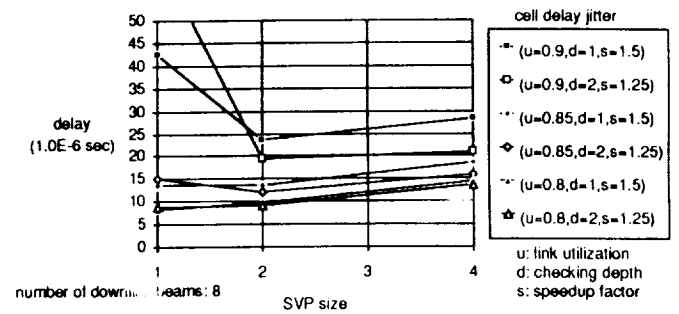


Figure 8: Cell Delay Jitter Versus SVP Sizes for Different Link Utilization, Checking Depth, and Speedup Factors



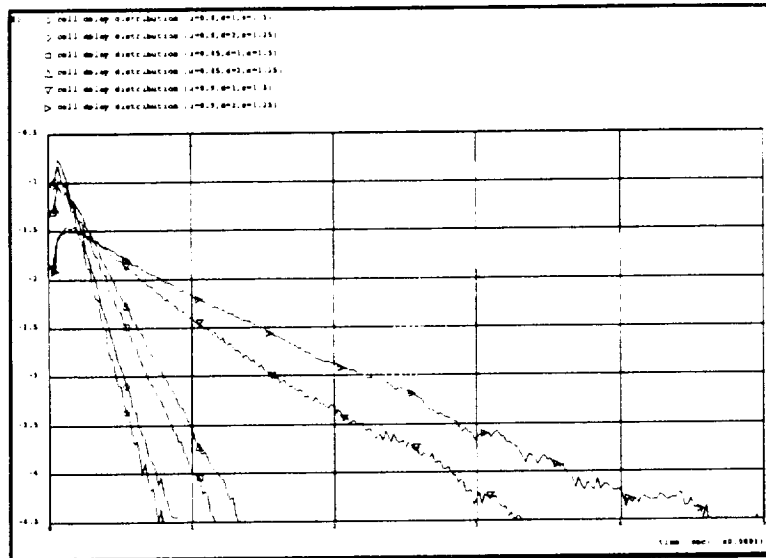


Figure 9: Single Cell Delay Distribution through the On-Board Switch for Different Utilizations, Checking Depth, and Speedup Factors

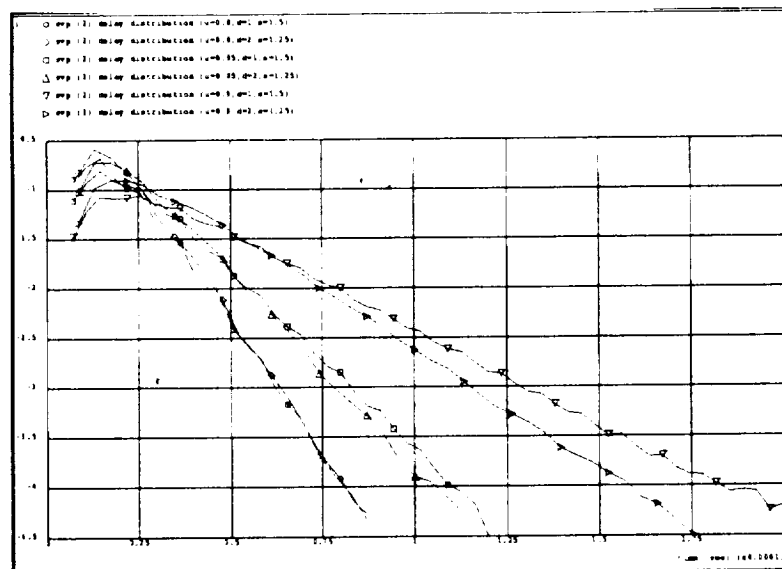


Figure 10: SVP Delay Distribution through the On-Board Switch for Different Utilizations, Checking Depth, and Speedup Factors When SVP Size is 2

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